

University of Bahrain
College of IT
Department of CE

Computer Architecture (ITCE 321)
Academic Year: 2015-2016
Semester: I
Test 1

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11-11-2015

Time: 1 Hour

Student I

Student I

Section:

Question	Points Attached
1 (43 marks)	40
2 (9 marks)	7
3 (15 marks)	13
(67 marks)	60

No mobile

Answer all questions.

YOU CAN ASSUME WHAT EVER YOU WANT!!

Q1

Answer the following questions:

1- The processor state of the MC68000 processor is:

(4 marks)

PC <31...0> Program counter, only 24 bits is used of it.
 IR <15...0> Instruction register with 16 bits.
 D [7...0] <31...0> data registers (7 registers each 32 bits)
 A [7...0] <31...0> address registers (7 registers each 32 bits)
 Status <15...0> user and program status

4

2- Dhrystone is defined as:

(2 marks)

a program used to measure performance of a computer.

1

3- The pre-fetching property of a processor means:

(2 marks)

fetch the next instruction to be executed, before the previous one completes executing.

2

The instructions fetched are kept in a queue. So the limitation here is size of queue.

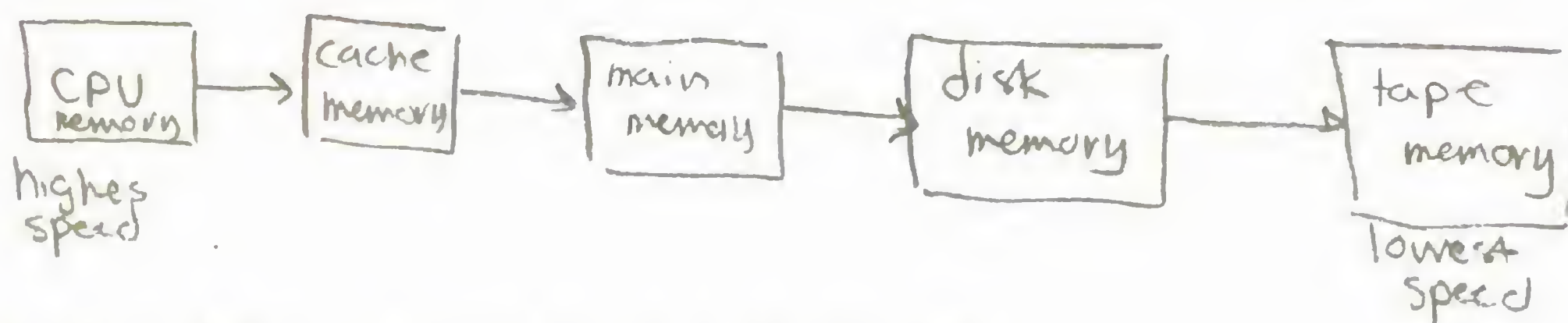
4- What is the meaning of the following RTN notations:

(5 marks)

RTN	Meaning
;	The instructions are executed in sequence. after the first complete, the next start.
:	The instructions on LHS and RHS can be executed at the same time.
←	assign value.
→	then (in condition)
<>	number of bits
@	duplication, Replication
[]	index
#	Concatenation
:=	naming - what's on RHS is description of LHS
()	to determine type (e.g sign) of arithmetic, or how short numbers are extended to longer (2's complement)

5

5- What is the hierarchy definition of data transfer? Give an example? (2 marks)



If the disk wants to read from CPU,
then the CPU makes its speed less to be compatible with the speed of disk memory
- The hierarchy is useful to determine the speed and space.

6- Express the RTN of both interpretation and execution of an SRC instruction. (3 marks)

run \wedge start \rightarrow run \leftarrow 1

if it is not run and start
then assign 1 to run

run \rightarrow IR \leftarrow M[PC] : PC \leftarrow PC + 4

if it is run

then put the content of the address of next instruction
to be executed in instruction register IR
and at the same time increment (PC) program
counter by 4.

7- Find the RTN and the corresponding addressing mode of each of the following instructions: (12 marks)

	Instruction	RTN	Addressing Mode
1	ld r1, 32	$R[r_1] \leftarrow M[32]$	direct
2	ld r32, 25(r8)	$R[r_{32}] \leftarrow M[25 + R[r_8]]$	displacement
3	st r3, 0(r7)	$M[0 + R[r_7]] \leftarrow R[r_3]$	displacement register indirect
4	la r8, 32	$R[r_8] \leftarrow 32$	immediate direct
5	ldr r13, -32	$R[r_{13}] \leftarrow M[PC - 32]$	relative
6	lar r8, 0	$R[r_8] \leftarrow M[PC]$	register relative

8- What are the components of the data path? (2 marks)

- arithmetic
- storage cells
- their connections

9- Write the RTN of the following SRS instructions:

(6 marks)

Instruction	RTN
Shra (:=op=27)	$R[r_a] \langle 31..0 \rangle \leftarrow n @ R[r_b] \langle 31 \rangle \# R[r_b] \langle 31..n \rangle$
shl (:=op=28)	$R[r_a] \langle 31..0 \rangle \leftarrow R[r_b] \langle 31..n..0 \rangle \# n @ 0$
shc (:=op=29)	$R[r_a] \langle 31..0 \rangle \leftarrow R[r_b] \langle 31..n..0 \rangle \# R[r_b] \langle 31..32..n \rangle$

6

10- The main disadvantage of using brl over br instruction is:

(2 marks)

brl will consume more area which means more power consumption, because it will store the content of PC registers first in another register, then it will branch to the specified register in the instruction.

11- Given that $IR \langle 31..0 \rangle \leftarrow Mem[x] \# Mem[x+1]$, then, the number of bits of each memory location is -----16-----bits.

(3 marks)

3

Q2:

Consider the following expression:

$$A = [Z - YM]^3$$

i. Evaluate the following expression using:

(6 marks)

- 1.
- 2.

4- address machine
Load/Store machine

op / result / op1 / op2 / address of next instruction
st a, [r]

Assuming that A, M, Y, Z are stored in the memory.

4- address machine	Load/Store machine
mpy A, Y, M, 105 sub A, A, Z, 209 mpy A, A, A, 313 mpy A, A, A, 417	ld r1, Z ld r2, Y ld r3, M mpy r4, r2, r3 sub r5, r1, r4 mpy r5, r5, r5 mpy r5, r5, r5 st A, r5

6

ii. The memory access time of:

(3 mark)

(4- address machine) = ~~9~~ x 4 = 36 times

mpy A, Y, M, ~~105~~
1 2 3 4 5
9 8 7 6

(Load/Store machine) = ~~(3x5) + 5 + (7x4)~~ = 48 times

~~ld~~ ~~st~~ ~~mpy~~ ~~sub~~

~~ld r1, Z~~
1 2 3

~~back to read~~ ~~back to take val~~ for load & store 5 times

~~mpy r4, r2, r3~~
1 2 3 4

for mpy, sub 7 times

~~back to store~~ ~~back to take value~~

~~st A, r5~~
1 2 3

~~back to store~~ ~~back to take val~~

1 3 3 3 3

Q3:

$$ET = \underset{\substack{\text{Instruction} \\ \text{count}}}{IC} * \underset{\substack{\text{clock} \\ \text{per} \\ \text{instruction}}}{CPI} * \underset{\substack{\text{tau} \\ \text{width}}}{T}$$

$$f = \frac{1}{T}$$
$$T = \frac{1}{f}$$

A)

Consider the following machines:

(9 marks)

- 1- Machine A: Average CPI is = 4 cycles, Working frequency = 2Ghz
- 2- Machine B: Average CPI=3 cycles, Working frequency = 2.8 Ghz

If we execute a code that has 10000 instructions on both machines; calculate:

a- Execution time for machine A

$$ET = IC * CPI * T = 10000 * 4 * \frac{1}{2 \times 10^9}$$
$$= 2 \times 10^{-6}$$

b- Execution time for machine B

$$ET = IC * CPI * T = 10000 * 3 * \frac{1}{2.8 \times 10^9}$$
$$= 1.07 \times 10^{-6}$$

c- The speed up of B machine over A machine

$$\text{Speed up} = \frac{\text{max}}{\text{min}} = \frac{2 \times 10^{-6}}{1.07 \times 10^{-6}} = 1.87$$

$$\text{Speed up percentage} = \frac{\text{max} - \text{min}}{\text{min}} * 100 = 86.92 \%$$

B)

A digital computer has a memory unit with 32 bits word per location. The instruction set consists of 128 different operations. All instructions have an operations code part (opcode) and a memory address part. Each instruction is stored in one word of memory. (6 marks)

a. How many bits are needed for the opcode?

$$\therefore 128 = 2^7$$

\therefore 7 bits are needed for the opcode

b. How many Bits are left for the address part of the instruction?

$$32 - 7 = 25 \text{ bits}$$

c. What is the maximum allowable size for memory?

$$\text{The maximum allowable size} = 2^{32}$$